IC of a Low-Dispersion Timing Discriminator, Intended to Process Nanosecond Pulses

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Abstract

An IC of a timing discriminator, implemented with a bipolar semicustom array (SA), is considered. The IC is intended to process nanosecond pulses and optimized with respect to the value of propagation delay dispersion. The discriminator includes 3 comparators and 1 DAC. The results of simulating the whole circuit of the timing discriminator are presented, as well as the experimental testing data for separate units.

A comparison is made with similar designs and the prospects of futher circuit developments are discussed.

References

[1] E.V. Atkin, P.V. Khlopkov, D.I. Savelyev, V.S. Zhukov. *High-Speed Comparator with Low Dispersion of Propagation Delay* , The Second International Workshop on *Data Acquisition Systems for Neutron Experimental Facilities (DANEF'2000)*, June 5 - 7, 2000.